IN THE CLAIMS:

Please revise the claims to read as follows:

1. – 3. (Cancelled)

4. (Original) A circuit for calculating reciprocal values, comprising:

an input for receiving input data, the input data being partitionable into a plurality of segments;

a selector circuit for selecting one of the segments;

a look-up table coupled to the selector circuit for receiving the selected segment, the look-up table having stored therein pre-calculated values, the look-up table configured to provide a respective one of the pre-calculated values in response to the selected segment; and

a shifter circuit coupled to the look-up table, the shifter circuit configured to shift the respective one of the pre-calculated values according to a relative position of the selected segment within the input data to generate an approximate reciprocal value for the input data.

5. (Original) The circuit of claim 4, wherein the selector circuit is configured to select a non-zero segment of the input data to be provided to the look-up table.

6. (Original) The circuit of claim 4 further comprising a first 2's complement circuit for converting a negative input data into the input data.

7. (Original) The circuit of claim 6 further comprising a second 2's complement circuit for converting the approximate reciprocal value into a negative approximate reciprocal value.

8. (Currently amended) A method of calculating reciprocal values in a processing circuit, comprising:

storing in a memory unit a plurality of reciprocal values in a look-up table in association with a plurality of possible input values, wherein the plurality of input values comprise addresses of the memory unit;

receiving an input value, the input value having a larger bit-width than each of the possible input values;

partitioning the input value into a plurality of segments each having a bit-width corresponding to each of the possible input values;

selecting one of the segments and providing the selected one of the segments to the look-up table to retrieve a respective one of the reciprocal values; and

shifting the respective one of the reciprocal values according to a position of the selected one of the segments in relation to the input value to generate an approximate reciprocal value for the input data.

9. (Original) The method of claim 8, wherein the storing comprises:

storing the plurality of possible input values as indices of the look up table.

10. (Previously presented) The method of claim 8, wherein the memory unit is the memory unit of a programmable logic device.

11. – 22. (Cancelled)

23. (Currently amended) In a programmable logic device, a circuit for determining a mathematical function for an input value, the circuit comprising:

an input for receiving the input value;

a partitioning circuit for partitioning the input value into a plurality of segments;

a look-up table coupled to the input for receiving the input value, the look-up table comprising a plurality of storage addresses and a plurality of pre-determined values stored in association with the storage addresses, wherein the pre-determined values are determined according to the mathematical function and the storage addresses at which the pre-determined values are stored;

a matching circuit for matching ~~the segments~~ a selected segment of the input value to a respective one of the storage addresses;

a shifter circuit configured to shift the pre-determined values retrieved from the look-up table according to a relative position of the segment of the input valve that is matched to a storage address; and

an output for outputting ~~a respective one of~~ the pre-determined values ~~that corresponds to the respective storage address~~ from the shifter circuit.

24. (Original) The circuit of claim 23, wherein the addresses range from 0 to 255.

25. (Original) The circuit of claim 24, wherein the look-up table stores 256 pre-determined values for each of the storage addresses.

26. (Original) The circuit of claim 23, wherein the programmable logic device is a field programmable gate array (FPGA).

27. (Currently amended) A method of calculating reciprocal values in a processing circuit, comprising:

storing a plurality of reciprocal values in a look-up table in a memory unit in association with a plurality of possible input values;

receiving an input value, the input value having a larger bit-width than each of the possible input values;

partitioning the input value into a plurality of segments each having a bit-width corresponding to each of the possible input values;

selecting one of the segments and providing the selected one of the segments as an address to the look-up table in the memory unit to retrieve a respective one of the reciprocal values; and

shifting the respective one of the reciprocal values according to a position of the selected one of the segments in relation to the input value to generate an approximate reciprocal value for the input data.

28. (Previously presented) Apparatus for calculating reciprocal values, comprising:

means for storing a plurality of reciprocal values in a look-up table in a memory unit in association with a plurality of possible input values;

means for receiving an input value, the input value having a larger bit-width than each of the possible input values;

means for partitioning the input value into a plurality of segments each having a bit-width corresponding to each of the possible input values;

means for selecting one of the segments and providing the selected one of the segments to the look-up table to retrieve a respective one of the reciprocal values; and

means for shifting the respective one of the reciprocal values according to a position of the selected one of the segments in relation to the input value to generate an approximate reciprocal value for the input data.

29. (Previously presented) The apparatus of claim 28, wherein the plurality of possible input values are indices of the look up table.

30. (Currently amended) A circuit for determining a mathematical function for an input value, the circuit comprising:

an input for receiving the input value;

a partitioning circuit for partitioning the input value into a plurality of segments;

a look-up table coupled to the input for receiving the input value, the look-up table comprising a plurality of storage addresses and a plurality of pre-determined values stored in association with the storage addresses, wherein the pre-determined values are determined according to the mathematical function and the storage addresses at which the pre-determined values are stored;

a matching circuit for matching ~~the segments~~ a selected segment of the input value to a respective one of the storage addresses; and

a shifter circuit coupled to the look-up table, the shifter circuit configured to shift respective ones of the pre-determined values retrieved from the look-up table according to a relative position of the ~~segments~~ segment of the input value that ~~are~~ is matched to a

storage address.

31. (Previously presented) The circuit of claim 30, wherein the addresses range from 0 to 255.

32. (Previously presented) The circuit of claim 30, wherein the look-up table stores 256 pre-determined values for each of the storage addresses.

33. (Previously presented) The circuit of claim 30, wherein the circuit is implemented in a field programmable gate array (FPGA).